IN THE CLAIMS

The following listing of the claims is provided in accordance with 37 C.F.R. §1.121:

1. (currently amended) A method for optical and electrical isolation between adjacent integrated devices, the method comprising:

forming at least one trench through an exposed surface of a silicon carbide (SiC) or gallium nitride (GaN) semiconductor wafer by removing a portion of the semiconductor wafer material;

forming an electrically insulating layer on the sidewalls and the bottom of the at least one trench[[;]] , wherein forming an electrically insulating layer comprises growing or depositing an oxide layer on the sidewalls and the bottom of the at least one trench;

filling the at least one trench by conformally depositing an optically isolating material; and

planarizing the semiconductor wafer surface by removing the portion of the optically isolating material above the exposed surface of the semiconductor wafer.

2.-4. (canceled).

5. (original) The method according to claim 1, wherein the step of forming an electrically insulating layer comprises growing a silicon dioxide (SiO2) layer on the sidewalls and the bottom of the at least one trench.

6. (original) The method according to claim 1, wherein the step of forming an electrically insulating layer comprises growing or depositing a layer comprising at least one of hafnium oxide, scandium oxide, and silicon nitride on the sidewalls and the bottom of the at least one trench.

7. (original) The method according to claim 1, wherein the optically isolating material comprises an opaque material capable of being deposited conformally.

8. (original) The method of claim 7, wherein the optically isolating material can be deposited at a temperature below 500°C.

9. (original) The method according to claim 1, wherein the optically isolating material comprises one or more of:

low pressure chemical vapor deposition (LPCVD) polysilicon;

titanium;

aluminum; or

tungsten.

10. (original) The method according to claim 1, wherein the optically isolating material comprises polysilicon.

11. (original) The method according to claim 1, wherein the electrically insulating material comprises silicon dioxide and the optically isolating material comprises polysilicon.

12. (original) The method according to claim 1, wherein the at least one trench is located between a plurality of adjacent device sites.

13. (original) The method according to claim 1, wherein the step of forming at least one trench comprises selectively etching the semiconductor wafer with reactive ion etching (RIE) or an inductively coupled plasma (ICP) process.

14. (original) The method according to claim 1, wherein the step of planarizing the semiconductor wafer surface comprises:

oxidizing the portion of the optically isolating material above the exposed surface of the semiconductor wafer; and

removing the oxidized portion of the optically isolating material.

15. (original) The method according to claim 1, wherein the step of planarizing the semiconductor wafer surface comprises subjecting the portion of the optically isolating material above the exposed surface of the semiconductor wafer to an etching process.

16. (original) The method according to claim 1, wherein the step of planarizing the semiconductor wafer surface comprises subjecting the portion of the optically isolating material above the exposed surface of the semiconductor wafer to a chemical mechanical polishing (CMP) process.

17. (currently amended) A microelectronic device comprising:

at least two integrated devices, wherein the at least two integrated devices are located in a silicon carbide (SiC) or gallium nitride (GaN) substrate; and

at least one trench in the substrate, wherein the at least one trench physically separates the at least two integrated devices, and the inside of the at least one trench is coated with an electrically insulating material, and filled with an optically isolating material that is conformally deposited, and planarized by removing a portion of the optically isolating material above an exposed surface of the substrate[[.]] , wherein the electrically insulating material comprises an oxide layer.

18. (canceled).

19. (canceled).

20. (original) The microelectronic device according to claim 17, wherein the electrically insulating material comprises a thermally grown silicon dioxide.

21. (original) The microelectronic device according to claim 17, wherein the optically isolating material comprises a low pressure chemical vapor deposition (LPCVD) polysilicon.

22. (currently amended) The microelectronic device according to claim 17, wherein the electrically insulating material comprises one or more of:

~~silicon nitride;~~

hafnium oxide; or

scandium oxide.

23. (original) The microelectronic device according to claim 17, wherein the optically isolating material comprises one or more of:

low pressure chemical vapor deposition (LPCVD) polysilicon;

titanium;

aluminum; or

tungsten.

24. (original) The microelectronic device according to claim 17, wherein the optically isolating material comprises an opaque material that can be deposited conformally under 500°C.

25. (original) The microelectronic device according to claim 17, wherein the at least two integrated devices comprise photodiodes.

26. (original) The microelectronic device according to claim 17, wherein the at least two integrated devices comprise photoemitters.

27. (original) The microelectronic device according to claim 17, wherein the at least two integrated devices comprise an array of serially connected diodes working as a gate to an insulated gate bipolar transistor (IGBT) or a metal-oxide-semiconductor field effect transistor (MOSFET).